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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/828,556	04/05/2001	Anthony P. Mauro	010034	6493

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Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER	
FIELDS, COURTNEY D	

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H2

Office Action Summary	Application No.	Applicant(s)	
	09/828,556	MAURO ET AL.	
	Examiner	Art Unit	
	Courtney D. Fields	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (U.S. Patent No. 6,088,800) and in further view of King (U.S. Patent No. 6,212,576). As per claim 1, Jones et al. teaches a device for accelerating functioning of a software application having multi-layer, high overhead protocols, the device comprising: a first processor operating a software application having a multi-layer protocol (column 6, lines 12-29), a high performance processor configured to operate one layer of the multi-layer protocol according to a command from the first processor (column 6, lines 30-43), and a memory accessible to each of the first processor and the high performance processor for passing commands and data between the first processor and the high performance processor (column 6, lines 3-18). However, Jones et al. does not teach a digital signal processor. King teaches a multi-layer protocol high performance processor comprising a digital signal processor (column 2, lines 21-26) It would have obvious to one of ordinary skill in the art at the time of the invention to

combine Jones et al.'s system for accelerating encryption processing with King's multiplayer protocol which will allow a secure software applications.

As per claim 2, Jones et al. teaches the first processor operates a multi-layer security protocol (Column 5, lines 49-53).

As per claim 3, Jones et al. teaches the high performance processor is configured to operate a mathematical algorithm layer of the multi-layer protocol (column 7, lines 65-67, Column 8, lines 1-11).

As per claim 4, Jones et al. (as modified by King) teaches the high performance processor further comprises a digital signal processor (King, column 2, lines 21-26).

As per claims 5 and 6, Jones et al. (as modified by King) teaches the digital signal processor is further configured to operate a modular math function (column 8, lines 12-67).

As per claim 7, Jones et al. teaches a device for accelerating security protocols, the device comprising: a multi-layer security protocol having one or more of an encryption algorithm and an authentication algorithm (column 7, lines 19-25), a shared memory (column 7, lines 25-38), a processor coupled to the memory and operating a first portion of a predetermined one of the security protocols (column 7, lines 39-64), and a high performance processor coupled to the memory and operating a second portion of the predetermined one of the security protocols (column 7, lines 39-64).

Regarding claim 8, Jones et al. (as modified by King) teaches the high performance processor operates the second portion of the security protocol in response to a

command from the processor and returns an interrupt signal (King, column 7, lines 30-62).

Regarding claim 9, Jones et al. (as modified by King) teaches the high performance processor operates the second portion of the security protocol on data from the processor (King, column 7, lines 62-67, Column 8, lines 1-22).

Regarding claim 10, Jones et al. teaches the high performance processor operates the second portion of the security protocol using a modular math function (column 8, lines 12-67).

Regarding claim 11, Jones et al. teaches the processor passes the data to the high performance processor via the shared memory, and the high performance processor returns a result from operating the second portion of the security protocol to the processor via the shared memory (column 7, lines 25-38).

Regarding claim 12, Jones et al. teaches a circuit for partitioning a multi-layer security services protocol, the circuit comprising: a shared memory (column 7, lines 25-38), first and second processor cores coupled to the shared memory, a multi-layer security services protocol partitioned between each of the first and second processor cores (column 7, lines 39-64), one or more application program interfaces operated by the first processor core for interfacing between the security services protocol and the second processor core (column 17, lines 7-12), and a modular math function operating on the second processor core (column 8, lines 12-67).

Regarding claim 13, Jones et al. teaches the first and second processor cores are coupled together through the shared memory (column 7, lines 25-38).

Regarding claim 14, Jones et al. teaches the security services protocol further comprises one of an encryption algorithm and an authentication algorithm (column 7, lines 19-25)

Regarding claim 15, Jones et al. teaches a method for accelerating a multi-layer protocol, the method comprising: partitioning a function of a multi-layer protocol in a first processor, distributing the function to a second high performance processor via a memory shared by both the first and second processors, performing the distributed function in the high performance processor (column 6, lines 44-67, Column 7, lines 1-14), and returning a result of the distributed function from the high performance processor via the shared memory (column 7, lines 25-38).

Regarding claim 16, Jones et al. teaches the distributed function further comprises performing the distributed function in response to a command from a first processor. (column 13, lines 7-32)

Regarding claim 17, Jones et al. teaches the first processor performs the partitioning of the function. (column 9, lines 41-62)

Regarding claim 18, Jones et al. teaches performing the distributed function comprises operating an algorithm to perform the function. (column 15, lines 39-55, Column 16, lines 47-51)

Regarding claim 19, Jones et al. teaches the algorithm is a modular math function. (column 8, lines 12-67)

Regarding claim 20, Jones et al. teaches the multi-layer protocol is a security layer. (Column 5, lines 49-53)

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Barrett, "Implementing the Rivest, Shamir, and Adleman Public Key Encryption Algorithm on a Standard Digital Signal Processor".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Courtney D. Fields whose telephone number is 571-272-3871. The examiner can normally be reached on Mon - Thurs. 6:00 - 4:00 pm; off every Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on 571-272-3868. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cdf
March 20, 2005

Andrew Caldwell

ANDREW CALDWELL
SUPERVISORY PATENT EXAMINER